REMARKS

Applicants have studied the Office Action dated June 9, 2003 and have made amendments to the claims. It is submitted that the application, as amended, is in condition for allowance. By virtue of this amendment, claims 1-9 and 18-28 are pending. Claims 1, 3, 5, 6, and 8 have been amended, and new claims 18-28 have been added. Reconsideration and allowance of the pending claims in view of the above amendments and the following remarks are respectfully requested.

Claims 1-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yamanaka (U.S. Patent No. 5,998,862). Claims 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamanaka in view of Herbst (U.S. Patent No. 5,913,110). These rejections are respectfully traversed.

The present invention is directed to improved injection molds that can be used to fabricate semiconductor packages containing an integrated circuit chip encapsulated in an encapsulation material. One preferred embodiment provides an injection mold for encapsulating an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip. The injection mold includes at least one injection cavity defined by a wall, and an insert. The injection cavity is able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material.

The insert has a front part that forms a first portion of the wall of the injection cavity and a transverse surface that lies parallel to one face of the chip. The transverse surface of the insert has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert. Because the front part of the insert forms a portion of the wall of the injection cavity, it is possible to manufacture a cavity having a wall with a normal roughness and to have a much lower roughness only on the transverse face of the insert. This is easier and less costly than carrying out a polishing operation on the wall of the cavity.

The Yamanaka reference is directed to semiconductor devices with a hollow package structure and a plastic lid. However, Yamanaka does not discloses an injection mold for encapsulating an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip, with the injection mold including at least one injection cavity able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material, and an insert having a front part that forms a first portion of the wall of the injection cavity and a transverse surface that has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert, as is recited in amended claim 1.

Yamanaka discloses hollow package semiconductor devices that use a plastic lid. More specifically, in the devices of Yamanaka, a chip 2 and lead frames 24 are affixed to a pedestal 21, as shown in Figures 3A-3H. The chip 2 is wire bonded to the lead frames 24. A transparent plastic lid 29 is affixed to the pedestal 21 so as to leave a cavity (or hollow portion) between the chip 2 and the inner surface 30 of the lid 29. The lid includes a light-transmission portion 29a that corresponds to the front surface of the chip 2, and the remainder of the lid is a light-non-transmission portion 29b. Thus, Yamanaka discloses a semiconductor package having a hollow portion between a chip that is attached to a pedestal and a plastic lid that has a light-transmission portion.

In contrast, preferred embodiments of the present invention provide an injection mold for encapsulating an integrated circuit chip in an encapsulation material. The injection mold includes at least one injection cavity that is defined by a wall and that is able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material. Additionally, the injection mold includes an insert having a front part that forms a first portion of the wall of the injection cavity and a transverse surface that lies parallel to one face of the chip and that has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert.

Yamanaka does not teach or suggest an injection mold for encapsulating an integrated circuit chip in an encapsulation material. First, in the semiconductor packages disclosed in

Yamanaka, the chip is attached to a pedestal and covered by a plastic lid so as to leave a hollow portion between the chip and the lid. The chip is not encapsulated in a block of encapsulation material. Thus, Yamanaka cannot even disclose an injection mold for encapsulating an integrated circuit chip in an encapsulation material, let alone an injection cavity that is able to receive encapsulation material so as to encapsulate the chip in a block of the encapsulation material.

Additionally, while Yamanaka teaches using injection molding at column 17, line 6 as pointed out by the Examiner, this only refers to the forming of the plastic lid. In particular, Figure 16A is a cutaway enlarged view of the semiconductor package of Figure 15B, and Figure 16B shows only the low-pass filter portion 80 of the plastic lid 82 of the same semiconductor package. The statement relied on by the Examiner only states that the low-pass filter portion 80 of the plastic lid 82 is formed by injection molding. After being formed by injection molding, the lid 82 is still affixed to the pedestal 78 so as to provide a hollow portion between the chip 2 that is attached to a pedestal 78 and the plastic lid 82 that has the low-pass filter portion 80, as shown in Figures 16A and 16D. The chip is not encapsulated in a block of encapsulation material, and Yamanaka does not teach or suggest using injection molding to encapsulate an integrated circuit chip in an encapsulation material. The use of injection molding to form a single plastic part (i.e., the lid) that is affixed to a pedestal to form a hollow package structure is not equivalent or comparable to using injection molding to encapsulate an integrated circuit chip in an encapsulation material so as to form a semiconductor package containing the chip.

Furthermore, even if the disclosure of using injection molding to form the plastic lid was sufficient to teach the general concept of using an injection mold to encapsulate an integrated circuit chip in an encapsulation material, Yamanaka still fails to disclose any structure whatsoever for the injection mold itself. At best, Yamanaka discloses the final product of the injection molding (i.e., the lid). Nowhere does Yamanaka teach or suggest using an injection mold that includes an injection cavity and an insert having a front part that forms a portion of the wall of the injection cavity and a transverse surface that has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert. Yamanaka does not disclose or suggest any injection mold for

forming the plastic lid, and thus cannot possibly disclose an injection mold having these claimed features. In fact, the Examiner recognizes that Yamanaka does not disclose an injection cavity of an injection mold by stating "(not shown)" next to this limitation in the Office Action. If Yamanaka fails to disclose an injection cavity, Applicants completely fail to understand how Yamanaka could possibly disclose an insert having a front part that forms a portion of the wall of the injection cavity.

Preferred embodiments of the present invention provide an injection mold for encapsulating an integrated circuit chip in an encapsulation material that includes at least one injection cavity able to house the chip and receive the encapsulation material so as to encapsulate the chip in a block of the encapsulation material, and an insert having a front part that forms a first portion of the wall of the injection cavity and a transverse surface that has a roughness that is chosen such that the face of the semiconductor package has a suitable roughness in a region corresponding to the transverse surface of the insert. Because the injection mold includes the insert whose front part forms a portion of the wall of the injection cavity, it is possible to manufacture a cavity having a wall with a normal roughness and to have a much lower roughness only on the transverse face of the insert. This is easier and less costly than carrying out a polishing operation on the wall of the cavity. Yamanaka does not even teach or suggest an injection mold for encapsulating an integrated circuit chip in an encapsulation material.

Applicants believe that the differences between Yamanaka and the present invention are clear in amended claim 1, which sets forth an injection mold according to one embodiment of the present invention. Therefore, claim 1 distinguishes over the Yamanaka reference, and the rejection of this claim under 35 U.S.C. § 102(b) should be withdrawn.

As discussed above, amended claim 1 distinguishes over the Yamanaka reference. Furthermore, the claimed features of the present invention are not realized even if the teachings of Herbst are incorporated into Yamanaka. Herbst does not teach or suggest the claimed features of the present invention that are absent from Yamanaka. Thus, amended claim 1 distinguishes over the Yamanaka and Herbst references, and thus, claims 2-9 (which depend from claim 1) also distinguish over the Yamanaka and Herbst references. Therefore, it is respectfully submitted that

the rejections of claims 1-9 under 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) should be withdrawn.

Claims 18-28 have been added by this amendment, and are provided to further define the invention disclosed in the specification. Claims 18-28 are allowable for at least the reasons set forth above with respect to claims 1-9.

In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

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